IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Sethuraman, R. et al.	CONFIRMATION NO. 4791 DOCK: NXP ID no. 81131478 (formerly NL020975)
SERIAL NO.:	10/530,495	EXAMINER: Jacob A. Petranek
FILED:	April 6, 2005	ART UNIT: 2183
FOR:	DATA PROCESSING APPARATUS ADDRESS RANGE DEPENDENT PARALLELIZATION OF INSTRUCTIONS	

APPEAL BRIEF TRANSMITTAL LETTER

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA. 22313-1450

Dear Sir:

Appellants respectfully submit three copies of an Appeal Brief for Appellants that includes an Appendix with the pending claims. The Appeal Brief is now due on January 21, 2009.

Applicant note that a prior Appeal Brief filed on March 19, 2008 was reopened by the examiner, and as such, the previously paid appeal fee is respectfully requested to be applied to this new appeal. A difference between the increased fee ($540) and the amount previously paid ($510) is $30.00, which should be deducted from Deposit Account No. 502-470. Also, should this be erroneous, authorization is hereby given to charge Deposit Account No. 502-470 for any underpayment, or credit any overages.

Respectfully submitted,
Aaron Waxler
Registration No. 48,027

/Steve Cha/
By: Steve Cha
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Date: December 2, 2008

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	**Sethuraman, R.**
Application No.	:	**10/530,495**
Filed	:	**April 6, 2005**
For	:	**Data Processing Apparatus Address Range Dependent Parallelization of Instructions**

APPEAL BRIEF

On Appeal from Group Art Unit 2183

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Date: December 2, 2008

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TABLE OF CASES

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the present application, NXP, B.V. Corporation, and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-12 and 14-17 have been presented for examination. All of these claims are pending, stand finally rejected, and form the subject matter of the present appeal.

IV. STATUS OF AMENDMENTS

In response to the Final Office Action, dated September 24, 2008, applicant filed a Notice of Appeal was timely filed on November 21, 2008 and this Appeal Brief is being filed, with appropriate fee, within the period of response from the date of the Notice of Appeal. Applicant note that a prior Appeal Brief filed on March 19, 2008 was reopened by the examiner, and as such, the previously paid appeal fee is respectfully requested to be applied to this new appeal. A difference between the increased fee ($540) and the amount previously paid ($510) is $30.00, which is submitted herein.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention, as expressed primarily in independent claims 1, 14 and 15, of which claim 1 is representative of the subject matter claimed, represents a Very Large Instruction Work (VLIW) processor that executes operations in parallel during the same instruction cycle (see page 1, lines 7-8, Figure 1), wherein the length of the instructions word is dependent upon a range to which its address belongs (see page 2, lines 17-19). More specifically, claim 1 recites an instruction address generation circuit for outputting an instruction address, an instruction memory system (Figure 2, element 12) arranged to output an instruction word addressed by the instruction address, including at least one type of memory (Figure 2, elements 20, 22) suitable for a achieving a desired instruction cycle time wherein longer instruction words are contained within ranges of progressively shorter instruction words (page 6, lines 6-7, page 6, lines 27-32) associated with a corresponding memory type (page 6, lines 27-27), an instruction execution unit (Figure 2, element 14), arranged to process a plurality of instructions from the instruction work in parallel, a detection unit (Figure 2, element 16), arranged to detect in which of a plurality of ranges the instruction address lies (page 4, line33-page5, line 5), the detection unit being coupled to the instruction execution unit parallelizes processing of the instructions from the instruction word, dependent on a detected range (page 4, lines 7-8).

Claim 14 recites a method of programming a data processing apparatus comprising generating a program of machine instructions for the apparatus, identifying an inner loop of the program, (see page 6, lines 30-page 7, line 1), loading the program into the instruction memory system, said memory system includes at least one type of memory suitable for a achieving a desired instruction cycle time, (see page 6, lines 6-9

and page 10, lines 9-14)) so that instructions from the inner loop are loaded at memory locations with instruction addresses in a range of addresses for which the apparatus provides a higher degree of parallelism than another range of addresses, wherein longer instruction words are contained within memory ranges of progressively shorter instruction words and are associated with a corresponding memory type. (see page 11, lines 6-19).

Claim 15 recites a method of executing a program with a data processing apparatus, the method comprising using an instruction address to fetch an instruction word, executing instructions from the fetched instruction word, detecting in which of a plurality of ranges the instruction address list lies, controlling a way in which instruction execution is parallelized dependent on a detected range, wherein longer instruction words are contained within ranges of shorter instruction words and instructions words are stored in a type of memory to achieve a desired instruction cycle time. (see page 11, lines 20-32).

The remaining claims, which depend from respective independent claims, express further aspects of the invention.

VI. GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

The issues in the present matter are whether:

1. Claims 1-5, 7 and 15-17 are unpatentable over Fisher (USP no. 6, 026, 479) in view Jensen (USP no. 7, 149, 878) under 35 USC §103(a);

2. Claims 6 and 14 are unpatentable over Fisher (USP no. 6, 026, 479) in view Jensen (USP no. 7, 149, 878) and further in view of Lilja ("Exploiting the Parallelism Available in Loops," IEEE, pages 13-26, Feb. 1994) under 35 USC §103(a);

3. Claim 8-9 are unpatentable over Fisher (USP no. 6, 026, 479) in view Jensen (USP no. 7, 149, 878) and further in view of Maiyuran (USPPA no.2002/0129201) under 35 USC §103(a);

4. Claims 10 and 12 are unpatentable over Fisher (USP no. 6, 026, 479) in view Jensen (USP no. 7, 149, 878) and further in view of Sanches (USPPA no. 2002/0116596) under 35 USC §103(a); and

5. Claim 11 is are unpatentable over Fisher (USP no. 6, 026, 479) in view Jensen (USP no. 7, 149, 878) and further in view of Sanches (USPPA no. 2002/0116596) and further in view of Maiyuran (USPPA no. 2002/0129201) under 35 USC §103(a).

VII. ARGUMENT

I. Rejection of Claims 1-5, 7 and 15-17 Under 35 USC §103 in view of Fisher and Jansen

The rejection of claims 1-5, 7 and 15-17 is in error because the references, when combined, fail to show a limitation cited in independent claims.

Claims 1-5, 7 and 15-17 stand rejected under 35 USC 103(a) as being unpatentable over the combination of Fisher and Jensen. The Final Office Action states that "per claim 1, Fisher discloses a data processing apparatus …[and] failed to teach a detection unit … However, Jensen disclosed a detection unit, arranged to detect in which of a plurality of ranges the instruction address lies… The advantage of mode switching through detecting a range of addresses over Fisher's methods is that it allows for

eliminating mode switching instructions and reducing time consuming interrupts... " (see Final Office Action, page 3, section 9).

Difference Between the Claimed Invention and the Cited References

The instant invention, as expressed in claim 1, for example, teaches a data processing apparatus, the apparatus comprising an instruction address generation circuit for outputting an instruction address, an instruction memory system arranged to output an instruction word addressed by the instruction address, including at least one type of memory suitable for achieving a desired instruction cycle time wherein longer instruction words are contained within ranges of progressively shorter instruction words associated with a corresponding memory type, an instruction execution unit, arranged to process a plurality of instructions from the instruction work in parallel, and a detection unit, arranged to detect in which of a plurality of ranges the instruction address lies, the detection unit being coupled to the instruction execution unit parallelizes processing of the instructions from the instruction word, dependent on a detected range.

Fisher discloses an apparatus for switching a CPU mode between regions of high instruction and low instruction achieve a desired level of parallelism is in computer programs. Fisher refers to two memories and a switch to switch between accessing instructions in one memory or the other. Jensen discloses an architecture for changing instruction sets by comparison of current instruction execution address with boundary address register values.

In combining the teaching of Fisher and Jensen, the Office Action refers to Fisher disclosing using an instruction cache to store the instructions. The use of a memory

cache is for achieving faster memory access times so that instructions can be accessed faster than if they were fetched from main memory. Thus, the use of instruction caches reads upon the claimed invention (see Final Office Action, page 13, section 30).

However, contrary to the assertions made by the Examiner in rejecting the claims, neither Fisher nor Jensen teach or suggest that ordering of longer instructions contained within progressively shorter instructions and that the memory type for storing the instructions is selected to achieve a desired instruction cycle time, as is recited in the claims.

In order to establish a *prima facie* case of obviousness, three basic criteria must be met, 1. there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the reference teachings, 2. there must be a reasonable expectation of success; and 3. the prior art reference must teach or suggest all the claim limitations.

In this case, a *prima facie* case of obviousness has not been made as each of the elements recited in the claims is not disclosed by the combination of Fisher and Jensen. Specifically, neither Fisher nor Jansen disclose the progress reduction in the length of the words in the memories, as is recited in the claims.

Accordingly, the subject matter recited in each of the independent claims is not render obvious and applicant respectfully requests that the rejection be withdrawn.

No Motivation Exists for the Examiner's Proposed Modification

In rejecting claim 1, the Examiner acknowledges that Fisher fails to disclose mode switching through detected ranges of address and refers to Jensen for teaching this

element. The Examiner asserts that the use of address based mode switching would eliminate mode switching instructions and reduce time consuming interrupts. (see page 4, lines 20-22).

However, the incorporation of the teaching of Jensen into that of Fisher would render the device disclosed by Fisher unsuitable for its intended purpose. Fisher discloses an instruction level controller that causes a switch between a main memory and a mini-instruction memory. The instruction level controller receives an interrupt to determine whether to access the main cache memory or the min-instruction memory. (see for example, col. 6, lines 7-13 "[t]he instruction level controller 140 switches to a low ILP mode upon receiving a LOW ILP mode signal, such as an interrupt, a procedure call instruction designated as a low ILP call, or a predetermined 'gateway' instruction executed by the CPU 100.").

Hence, Fisher fails to provide any teaching regarding switching between one memory or another based on a memory address range and specifically refers to a controller to determine whether one memory or the other is to be accessed. This assess is based on the length of the instruction and not the memory address of the instruction.

For the above remarks, Applicant respectfully submits that the combined teachings of the references cited fails to render obvious the subject matter recited in independent claim 1, for example.

With regard to the dependent claims, these claims are dependent from independent claims 1 and, hence, are not rendered obvious by virtue of their dependency upon an allowable base claim.

Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

II. Rejection of the Remaining Claims

Claims 6 and 14 stand rejected under 35 USC §103(a) as being unpatentable over Fisher, Jensen and Lilja. Claim 8-9 stand rejected under 35 USC §103(a) are unpatentable over Fisher, Jensen and Maiyuran. Claims 10 and 12 stand rejected under 35 USC §103(a) as being unpatentable over Fisher, Jensen and Sanches. Claim 11 stands rejected under 35 USC §103(a) as being unpatentable over Fisher, Jensen, Sanches and Maiyuran.

With regard to the remaining claims, these claims depend from the independent claims. Applicant respectfully submits that these claims are allowable at least for their dependence upon allowable base claims, without even contemplating the merits of the dependent claims for reasons analogous to those held in *In re Fine*, 837 F.2d 1071, 5 USPQ 2d 1596 (Fed. Cir. 1988) (if an independent claim is non-obvious under 35 U.S.C. §103(a), then any claim depending therefrom is non-obvious).

In view of the above, applicant submits that the independent claims and the claims dependent therefrom are patently distinguishable and allowable over the teaching of the cited references.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Respectfully submitted,

Aaron Waxler
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/Steve Cha/

Date: December 2, 2008

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IX. CLAIMS APPENDIX

The claims which are the subject of this Appeal are as follows:

1. (Previously presented) A data processing apparatus, the apparatus comprising:

an instruction address generation circuit for outputting an instruction address;

an instruction memory system arranged to output an instruction word addressed by the instruction address, including at least one type of memory suitable for a achieving a desired instruction cycle time wherein longer instruction words are contained within ranges of progressively shorter instruction words associated with a corresponding memory type;

an instruction execution unit, arranged to process a plurality of instructions from the instruction work in parallel;

a detection unit, arranged to detect in which of a plurality of ranges the instruction address lies, the detection unit being coupled to the instruction execution unit parallelizes processing of the instructions from the instruction word, dependent on a detected range.

2. (Previously presented) A data processing apparatus according to claim 1, wherein the instruction execution unit and/or the instruction memory system is arranged to adjust a width of the instruction word that determines a number of instructions from the instruction word that is processed in parallel, dependent on the detected range.

3. (Previously presented) A data processing apparatus according to claim 1, wherein the instruction execution unit comprise a plurality of functional units, the instruction execution unit being arranged to select a subset of the functional units that is available for processing the instruction, dependent on the detected range.

4. (Previously presented) A data processing apparatus according to claim 1, wherein the instruction execution unit comprise a plurality of functional units, the instruction execution unit being arranged to select whether functional units or groups of functional units from a set of functional units each receive respective instructions from the instruction word, or receive a shared instruction from the instruction word, dependent on the detected range.

5. (Previously presented) A data processing apparatus according to claim 2, wherein the instruction memory comprise a first memory unit and a second memory unit, providing storage with a first and second unit of width of addressable memory locations for instructions words of different lengths with addresses in a first and second range respectively, the first and second unit of width being mutually different.

6. (Previously presented) A data processing apparatus of claim 5, programmed to execute a program, longer instruction words from a inner loop of the program being stored in the first memory unit, shorter instruction words from a majority of the program outside the inner loop being stored in the second memory unit, the first unit of width being larger that the second unit of width.

7. (Previously presented) A data processing apparatus according to claim 5, comprising a memory mapping unit arranged to map the instruction address onto the first memory unit or the second memory unit, dependent on the detected range.

8. (Previously presented) A data processing apparatus according to claim 5, wherein the instruction memory system is arranged to disable supply of clock signals to the first memory unit when addresses in the second range are detected.

9. (Previously presented) A data processing apparatus according to claim 5, wherein the instruction memory system is arranged to disable supply of clock signals to all but the memory unit from whose address range addresses are detected.

10. (Previously presented) A data processing apparatus according to claim 2, wherein the instruction memory system comprises a plurality of memory units, each arranged to be responsive to instruction addresses in a respective range, the instruction memory allowing partial overlap of the respective range, the instruction memory system being arranged to supply the instruction word as a combination of instructions from those of the memory units in whose respective range the instruction address lies.

11. (Previously presented) A data processing apparatus according to claim 10, wherein the instruction memory system is arranged to disable supply of clock signals to at least one of the memory units when the instruction address is not in the respective range of said at least one of the memory units.

12. (Previously presented) A data processing apparatus according to claim 10, wherein the execution unit comprises groups of one or more functional units, each group being coupled to a respective predetermined one of the memory units, for receiving instructions from the instruction words, when the instruction address is in the respective range of the respective predetermined one of the memory unit to which the group is coupled.

13. (Cancelled)

14. (Previously presented) A method of programming a data processing apparatus comprising:

generating a program of machine instructions for the apparatus;

identifying an inner loop of the program;

loading the program into the instruction memory system, said memory system includes at least one type of memory suitable for a achieving a desired instruction cycle time, so that instructions from the inner loop are loaded at memory locations with instruction addresses in a range of addresses for which the apparatus provides a higher degree of parallelism than another range of addresses, wherein longer instruction words

are contained within memory ranges of progressively shorter instruction words and are associated with a corresponding memory type.

15. (Previously presented) A method of executing a program with a data processing apparatus, the method comprising:

using an instruction address to fetch an instruction word;

executing instructions from the fetched instruction word;

detecting in which of a plurality of ranges the instruction address list lies,

controlling a way in which instruction execution is parallelized dependent on a detected range, wherein longer instruction words are contained within ranges of shorter instruction words and instructions words are stored in a type of memory to achieve a desired instruction cycle time.

16. (Previously presented) A method according to claim 15, the method comprising adapting a width of the fetched instruction word dependent on the detected range.

17. (Previously presented) A method according to claim 15, the method comprising changing a selection of functional units of the apparatus that is used to execute the instructions dependent on the detected range.

X. EVIDENCE APPENDIX

No further evidence is submitted herein.

XI. RELATED PROCEEDING APPENDIX

No related proceedings are pending and, hence, no information regarding same is available.